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| --- | --- | --- |
| Field Value | Description |  |
| dti | Dolphin Technology |  |
| sp | Single Port SRAM Block without redundancy | Default |
| spp | SinglePort Plus [with Column Redundancy] |  |
| sppp | Single Port Plus Plus [with Row Redundancy] |  |
| shd/hd/shc/hc | Bit cell type |  |
| ll | Low Leak- deep sleep |  |
| lli | Low Leak- light sleep | Optional |
| dr | Dual Power Rail | Optional |
| pg | Power gating | Optional |
| pgr | Power gating with data retention | Optional |
| Tm06/07 | Foundry = TSMC Technology = 06/07nm | Default |
| ffp/ffc | Process |  |
| od | Over Drive |  |
| hvt | Higher Threshold Voltage logic device | Optional |
| lvt | Low Threshold Voltage logic device | Optional |
| ulvt | Ultra low Threshold Voltage logic device | Optional |
| nw | Number of Words |  |
| ws | Word Size |  |
| secded | Single Error Correct Double Error Detect | Optional |
| sec | Single Error Correct | Optional |
| op | Odd Parity | Optional |
| ep | Even Parity | Optional |
| \* | Number of parity bits | Optional |
| i | Clock = Negative Edge. If not present, Clock = Positive Edge | Optional |
| t | BistMux is selected and Test Pins are generated. | Optional |
| x | XOR the outputs of the bist mux | Optional |
| aw | Asynchronous Write through is enabled. | Optional |
| 4 | Column Mux select Option 4 | Default for SP |
| 8 | Column Mux select Option 8 |  |
| 16 | Column Mux select Option 16 |  |
| 32 | Column Mux select Option 32 |  |
| bw | Bit Write |  |
| byw | Byte Write |  |
| ww | Global Write | Default |
| r | Registered Output | Optional |
| 1x | Output Driver Strength 1x | Default |
| 3x | Output Driver Strength 3x |  |
| 9x | Output Driver Strength 9x |  |
| oe | Output enable | Optional |
| r | Redundant Row(s) created | Optional |
| c | Redundant Column(s) created | Optional |
| pn | Power Ring Enabled | Optional |
| po | Power Ring Enabled with Overlap | Optional |
| isol | Isolation | Optional |